Amendments to the Claims

Please cancel claim 12 and amend claim 1 as shown in the following list of claims. This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (currently amended) A memory device comprising, in a single integrated circuit package:

a static memory means defining at least first and second nodes communicatively connected with read and/or write data lines, wherein the static memory means comprises a pair of cross-coupled inverters, each of the cross-coupled inverters including first and second transistors that are connected in series, sources of the first transistors of the cross-coupled inverters being connected to each other; and

at least one non-volatile memory means associated with said static memory means, and writing data stored therein to said static memory means; said non-volatile memory means comprising a first non-volatile element having a control gate connected to a first node and a source connected to a second node, and a second non-volatile element having a control gate connected to the second node and a source connected to the first node, the drain of each non-volatile element being connected by means of a respective transistor to a supply means; characterized in that said respective transistors are arranged to isolate the drains of the first and second non-volatile elements from the supply means during a program cycle of the memory device, the drains of the first and second non-volatile elements being connected to drains of the respective transistors, the supply means being connected to sources of the respective transistors, the sources of the respective transistors being also connected to the sources of the first transistors of the cross-coupled inverters

~~wherein the static memory means comprises a pair of cross-coupled inverters~~.

2. (previously presented) A memory device according to claim 1, wherein said non-volatile memory elements comprise embedded flash or EEPROM elements.

3. (previously presented) A memory device according to claim 1, wherein said non-volatile memory elements comprise double or single poly floating gate type memory cells.

4. (previously presented) A memory device according to claim 1, wherein said non-volatile memory elements comprise devices which can be programmed and erased by means of tunneling of charges.

5. (previously presented) A memory device according to claim 1, wherein the non-volatile memory elements are programmed with opposite data.

6. (canceled).

7. (previously presented) A memory device according to claim 1, wherein one or more respective selection transistors are provided, by means of which the nodes are communicatively coupled to the read and/or write lines.

8. (previously presented) A memory device according to claim 1, including one or more isolation transistors.

9. (previously presented) A reconfigurable programmable logic device including a memory device according to claim 1.

10. (previously presented) A field programmable gate array including a memory device according to claim 1.

11. (previously presented) A memory device according to claim 1, wherein gates of the respective transistors are connected together to receive a common signal.

12. (canceled).